

CLAIMS

What is claimed is:

1 1. A method of input offset voltage compensation in a
2 bipolar transistor differential amplifier having resistive
3 loads on the bipolar transistor differential input pair
4 comprising:

5 biasing the differential input pair with a bias current
6 proportional to absolute temperature;

7 splitting the resistive loads into series combinations
8 of a primary resistance and a trim resistance;

9 coupling a trim current source output to a trim
10 resistances, the trim current source comprising a plurality
11 of proportional to absolute temperature current source
12 components individually controllably switchable to the trim
13 current source output, each contributing a respective trim
14 current component to the trim current source in a binary
15 progression; and,

16 switching selected proportional to absolute temperature
17 current source components to the trim current source output
18 to minimize the input offset voltage of the differential
19 amplifier.

1 2. The method of claim 1 wherein the plurality of
2 proportional to absolute temperature current source

3 components are equal current components proportional to the
4 current biasing the differential input pair, each current
5 source component being switchable to a respective node of an
6 R-2R network.

1 3. The method of claim 2 wherein switching selected
2 proportional to absolute temperature current source
3 components to the trim current source comprises loading a
4 switch control word into a control register, each bit of the
5 control word controlling a respective switch.

1 4. The method of claim 3 wherein the control word is
2 provided through a digital interface.

1 5. The method of claim 1 further comprised of coupling
2 the trim current source output to a predetermined one of the
3 trim resistances, coupling a crossover switch in series with
4 the resistive loads, and controlling the crossover switch to
5 predetermine which trim resistance requires trim current for
6 input offset voltage compensation.

1 6. The method of claim 1 wherein the differential
2 amplifier includes a symmetrical high gain second stage and
3 further comprising biasing the second stage with a constant
4 current.

1 7. The method of claim 1 wherein the differential
2 amplifier includes a symmetrical high gain second stage and
3 further comprising biasing the second stage with a current
4 proportional to absolute temperature.

1 8. A method of input offset voltage compensation in a
2 bipolar transistor differential amplifier having resistive
3 loads on the bipolar transistor differential input pair
4 comprising:

5 biasing the differential input pair with a bias current
6 proportional to absolute temperature;

7 coupling a trim current source output to at least one of
8 the resistive loads, the trim current source comprising a
9 plurality of proportional to absolute temperature current
10 source components individually controllably switchable to the
11 trim current source output; and,

12 switching selected proportional to absolute temperature
13 current source components to the trim current source output
14 to minimize the input offset voltage of the differential
15 amplifier.

1 9. The method of claim 8 wherein switching selected
2 proportional to absolute temperature current source
3 components to the trim current source comprises loading a

4 switch control word into a control register, each bit of the
5 control word controlling a respective switch.

1 10. The method of claim 9 wherein the control word is
2 provided through a digital interface.

1 11. The method of claim 8 further comprising splitting
2 the resistive loads into series combinations of a primary
3 resistance and a trim resistance, and coupling the trim
4 current source output to at least one of the trim
5 resistances.

1 12. The method of claim 8 wherein the proportional to
2 absolute temperature current source components contribute
3 respective trim current components to the trim current source
4 in a binary progression.

1 13. The method of claim 12 wherein the plurality of
2 proportional to absolute temperature current source
3 components are equal current components proportional to the
4 current biasing the differential input pair, each being
5 switchable to a respective node of an R-2R network.

1 14. The method of claim 8 further comprised of coupling
2 a crossover switch in series with the resistive loads and
3 controlling the crossover switch to predetermine the initial
4 polarity of the input offset voltage to be compensated.

1 15. The method of claim 8 wherein the differential
2 amplifier includes a symmetrical high gain second stage and
3 further comprising biasing the second stage with a constant
4 current.

1 16. The method of claim 8 wherein the differential
2 amplifier includes a symmetrical high gain second stage and
3 further comprising biasing the second stage with a current
4 proportional to absolute temperature.

1 17. In a bipolar transistor differential amplifier, the
2 improvement comprising:

3 a bipolar transistor differential input pair, each
4 transistor having as a load a series combination of a primary
5 resistance and a trim resistance;

6 a proportional to absolute temperature current source
7 biasing the differential input pair; and,

8 a trim current source having an output coupled to at
9 least one of the trim resistances, the trim current source
10 comprising a plurality of proportional to absolute
11 temperature current source components individually
12 controllably switchable to the trim current source output,
13 each contributing a respective trim current component to the
14 trim current source in a binary progression.

1 18. The improvement of claim 17 further comprising an
2 R-2R network and wherein the plurality of proportional to
3 absolute temperature current source components are equal
4 current components proportional to the current biasing the
5 differential input pair, each being switchable to a
6 respective node of the R-2R network.

1 19. The improvement of claim 18 further comprising a
2 register holding a control word controlling the switching of
3 individual proportional to absolute temperature current
4 source components.

1 20. The improvement of claim 19 further comprising a
2 digital interface coupled to the register for inputting a
3 control word to the register.

1 21. The improvement of claim 17 further comprised of a
2 crossover switch in series with the resistive loads, a
3 control word in the control register also controlling the
4 crossover switch.

1 22. The improvement of claim 17 further comprising a
2 symmetrical high gain second stage biased with a constant
3 current.

1 23. The improvement of claim 17 further comprising a
2 symmetrical high gain second stage biased with a current
3 proportional to absolute temperature.

1 24. In a bipolar transistor differential amplifier, the
2 improvement comprising:

3 a bipolar transistor differential input pair, each
4 transistor having a resistive load;

5 a proportional to absolute temperature current source
6 biasing the differential input pair; and,

7 a trim current source having an output coupled to at
8 least one of the resistive loads, the trim current source
9 comprising a plurality of proportional to absolute
10 temperature current source components individually
11 controllably switchable to the trim current source output,
12 each contributing a respective trim current component to the
13 trim current source.

1 25. The improvement of claim 24 further comprising a
2 register holding a control word controlling the switching of
3 individual proportional to absolute temperature current
4 source components.

1 26. The improvement of claim 25 further comprising a
2 digital interface coupled to the register for inputting a
3 control word to the register.

1 27. The improvement of claim 24 wherein at least one
2 resistive load comprises a series combination of a primary
3 resistance and a trim resistance, the trim current source
4 output being coupled to at least one of the trim resistances.

1 28. The improvement of claim 24 wherein the
2 proportional to absolute temperature current source
3 components each contribute a respective trim current
4 component to the trim current source in a binary progression.

1 29. The improvement of claim 24 further comprising an
2 R-2R network and wherein the plurality of proportional to
3 absolute temperature current source components are equal
4 current components proportional to the current biasing the
5 differential input pair, each being switchable to a
6 respective node of the R-2R network.

1 30. The improvement of claim 24 further comprised of a
2 crossover switch in series with the resistive loads and
3 controlling the crossover switch to predetermine which
4 resistive load is coupled to which compensated bipolar
5 transistor.

1 31. The improvement of claim 24 further comprising a
2 symmetrical high gain second stage biased with a constant
3 current.

1 32. The improvement of claim 24 further comprising a
2 symmetrical high gain second stage biased with a current
3 proportional to absolute temperature.